REMARKS

Claims 1-20 have been presented for examination in the above-identified U.S. Patent Application.

Claims 1-20 have been rejected in the Office Action dated March 12, 2007, the rejection of the Claims being made final.

Claims 1, 3, 6, 8, 12, 13, 17, 19, and 20 have been amended by this Amendment B.

Claims 4, 7, 15 and 15 have been cancelled by this Amendment B.

Claims 1-3, 5, 6, 8-13 and 16-20 are still in the application and reconsideration of the Application is hereby respectfully requested.

Examiner has maintained the rejection provided in the Office Action dated September 13, 2006. In that Office Action, Claims 1-20 were rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Publication No. 2002/0184477 issued in the name of Swaine (hereinafter referred to as Swaine).

Before addressing the rejection as indicated by Examiner, the invention sought to be protected by the amended Application of the present Continuation Application will be summarized. The invention involves an address

comparator unit, each comparator unit including a first and a second comparator. The two comparators of the comparator unit are interconnected so that a positive output signal will be generated only when the two conditions defined by both comparators are identified as providing positive comparison result with the control signals. This result is accomplished by interconnecting the output signals of the two comparators so that a positive output signal is provided only when the conditions defined by control signals in the two comparator units are present. Note that the present invention includes a further level of generality, i.e., the two comparators may operate on the same address or on two addresses. These features are present in the independent Claims 1, 6, 12, and 17 as amended. In addition each of the independent Claims includes a qualifying circuit that enables the two comparators only when the target processor is in the appropriate state.

Referring now to the Swaine reference, this reference has several elements similar of the present invention. However, the present invention includes, in each of the independent Claims, the inter-connection between the two comparators of the comparator unit. This configuration is not found in the Swaine reference. Clearly, this is not a matter of design choice. One address can for example be the program counter (address) and the second address can be the address designated by the program counter (address). Further, the use of two comparators in a comparator unit permits an address to be analyzed for two characteristics as well as identifying relationships in two separate

addresses. In the (0022) paragraph cited by Examiner in the final rejection, the use of a multiplexer is described as selecting an output between a comparator and a "context identifier comparators". Nowhere is there found in the Swaine reference an inter-connection between comparators (cf Fig. 3 of the Swaine reference).

In view of this physical difference between the Swaine reference and the present invention (i.e., the inter-connection between two comparators in a comparator unit), the rejection under 35 U.S.C. 102(e) over Swaine is respectfully traversed.

In addition, because of the additional flexibility of comparator unit described in the application, rejection under 35 U.S.C. 103(a) over Swaine is respectfully traversed.

CONCLUSION

In view of the foregoing discussion and the foregoing amendments, it is believed that Claims 1-3, 5, 6, 8-13 and 16-20 are now in condition for allowance and allowance of Claims 1-3, 5, 6, 8-13 and 16-20 is respectfully requested. Applicant hereby respectfully requests a timely Notice of Allowance be issued for this Application.

Respectfully submitted,

William W. Holloway
Attorney for Applicant(s)
Reg. No. 26,182

Texas Instruments Incorporated
PO Box 655474, MS 3999
Dallas, TX 75265
(281) 274-4064
Dated: July 3, 2007